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EXAMINER	
DANIELS, ANTHONY J	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,366	UYA, SHINJI	
	Examiner	Art Unit	
	Anthony J. Daniels	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/31/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,15 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8,11,12,15 and 16* is/are rejected.

7)☒ Claim(s) *4,5,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment, filed 5/31/2005, has been entered and made of record. Claims 1-12,15,16 are pending in the application.

2. The amendments to the title and drawings have overcome the examiner's objection.

Response to Arguments

3. It is respectfully submitted that the amendments to claims 11,15 have not overcome the cited prior art in the previous Office Action. Examiner's remarks can be found in the context of the rejections that follow.

4. Applicant's arguments with respect to claims 1-3,6-8 have been considered but are moot in view of the new ground(s) of rejection.

5. Applicant's arguments filed 5/31/2005 with respect to claims 12,16 have been fully considered but they are not persuasive. In regard to applicant's remarks (p. 20, 103 rejections), the examiner disagrees. On p. 20, last paragraph, applicant contends, "...the Examiner merely states that the motivation for combining the references is found in certain advantages stated by the Examiner (see, e.g., Office Action at pp. 14-15). The Examiner, however, indicates nothing from within the applied references to evidence the desirability of this combination. This is an insufficient showing of motivation..." It is submitted that the examiner, **on p. 16** (first

paragraph), has used explicit teaching from the **applied reference**, Tanaka et al. (US # 6,559,889), to show motivation for the combination (see Non-Final Rejection, p. 16, first paragraph; "...it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor substrate of Udagawa et al. to include a p-type well region that determines the amount of charge accumulable in each photosensor, **because one of ordinary skill in the art would recognize that this would allow the saturation signal charge amount to increase or decrease in anticipation of reduction, thereby preventing such characteristics as S/N ratio and dynamic range from being deteriorated due to the reduction of saturation signal charge amount (Tanaka et al., Col. 7, Lines 51-62)...**".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 11,15 are rejected under 35 U.S.C. 102(b) as being anticipated by Udagawa et al. (US # 5,880,781).

As to claim **11**, Udagawa et al. teaches a solid-state image pickup device (see Figure 1, Figure 2A; Col. 4, Lines 30-34; *{The color layout of Figure 1 is used on the CCD of Figure 2A.}*), comprising: a semiconductor substrate (*The semiconductor substrate is an inherent part of*

a CCD.) having a two-dimensional plane on a surface thereof (see Figure 1, Figure 2A; Col. 4, Lines 30-34; *{The color layout of Figure 1 is used on the CCD of Figure 2A.}*); a plurality of photoelectric converter elements arranged in the two-dimensional plane in a matrix configuration having rows and columns (see Figure 1; Col. 4, Lines 35,36); an array of color filters including a plurality of units (Figure 1, Figure 2A, rows starting C1 and M1 (one unit); rows starting C3 and G3 (another unit)), each unit consisting of two adjacent photoelectric converter element rows (see Figure 1; rows starting C Y C and M G M are adjacent, the same for rows starting C3 and G3), said units being repeatedly and contiguously arranged in said array in a column direction (see Figure 1, Figure 2A, Col. 3, Lines 14-17, the units are contiguous as can be seen in Figure 1 and Figure 2A) in which one color filter of the array is formed over each of said photoelectric converter elements (Figure 1), wherein, the first row of each unit has a first color layout of color filters arranged in a row direction (see Figure 1; row starting C Y C) and the second row of each unit has a row of a second color layout of color filters arranged in the row direction (see Figure 10, row starting M G M), said second color layout being different from said first color layout (see Figure 1; *{C Y C is different from M G M.}*); one vertical charge transfer channel region formed in said semiconductor substrate for each of the columns of said photoelectric converter elements, adjacent to said each column (see Figure 2B; Col. 4, Lines 36,37, "...VCCD."); a plurality of vertical charge transfer electrodes in which two vertical charge transfer electrodes are disposed over said vertical charge transfer channel regions for each of the rows of said photoelectric converter elements (see Figure 2A, V1, V2; *{The gates V1 and V2 are used for the single row of pixels starting with C1; pulses are applied to the row starting C1, so it is inherent that there is some sort of electrical connection disposed over the charge transfer*

region.}.}); and a drive circuit capable of applying readout pulse voltages (see Figure 3, CCD Driver "3"; Col. 4, Lines 64-67) to said vertical charge transfer electrodes corresponding to said photoelectric converter element row having said first color layout in a first unit (see Figure 2A; *{V1-V4 are applied to rows starting C1 and M1.}*) and to said vertical charge transfer electrodes corresponding to said photoelectric converter element row having said second color layout in a second unit (see Figure 2A; *{V1-V4 are applied to rows starting C3 and G3.}*), said second unit being at a position apart from said first unit by two photoelectric converter element rows in the column direction (see Figure 2A; *{The **two** rows starting Y2 and G2 separate the first unit (C1 and M1) and the second unit (C3 and G3)}*).

As to claim **15**, Udagawa et al. teaches a method of controlling a solid-state image pickup device (see Figure 1, Figure 2A; Col. 4, Lines 30-34*; {The color layout of Figure 1 is used on the CCD of Figure 2A.}*), comprising a semiconductor substrate (*The semiconductor substrate is an inherent part of a CCD.*) having a two-dimensional plane on a surface thereof (see Figure 1, Figure 2A; Col. 4, Lines 30-34; *{The color layout of Figure 1 is used on the CCD of Figure 2A.}*); a plurality of photoelectric converter elements arranged in the two-dimensional plane in a matrix configuration having rows and columns (see Figure 1; Col. 4, Lines 35,36); an array of color filters including a plurality of units (Figure 1, Figure 2A, rows starting C1 and M1 (one unit); rows starting C3 and G3 (another unit)), each unit consisting of two adjacent photoelectric converter element rows (see Figure 1; rows starting C Y C and M G M are adjacent, the same for the unit of rows C3 and G3), said units being repeatedly and contiguously arranged in said array in a column direction (see Figure 1, Figure 2A; Col. 3, lines 14-17, the units are contiguous as can be seen in Figure 1 in the column direction), in which one color filter of the array is formed

over each of said photoelectric elements (Figure 1, Figure 2A), wherein, the first row of each unit has a first color layout of color filters arranged in a row direction (see Figure 1, row starting C Y C; Col. 4, Lines 30-34) and the second row of each unit has a second color layout of color filters arranged in the row direction, said second color layout being different from said first color layout (see Figure 1, row starting M G M different from row starting C Y C); one vertical charge transfer channel region formed in said semiconductor substrate for each of the columns of said photoelectric converter elements, adjacent to said each column (see Figure 2B; Col. 4, Lines 36,37, "...VCCD."); a plurality of vertical charge transfer electrodes in which two vertical charge transfer electrodes are disposed over said vertical charge transfer channel regions for each of the rows of said photoelectric converter elements (see Figure 2A, V1, V2,V3,V4, etc.; *{The gates V1 and V2 are used for the single row of pixels starting with C1; and as can be seen from Figure 2A, there are two electrodes for each row continuing down the set.}*); and a drive circuit capable of applying readout pulse voltages (see Figure 3, CCD Driver "3"; Col. 4, Lines 64-67) to said vertical charge transfer electrodes corresponding to said photoelectric converter element row having said first color layout in a first unit (see Figure 2A; V3 and V4 belonging to the row starting M1) succeeding one after another in a column direction (see Figure 1; Col. 3, Lines 14-17) and to said vertical charge transfer electrodes corresponding to said photoelectric converter element row (see Figure 2A; V1 and V2 belonging to C3) having said second color layout in a second unit (see Figure 2A, C3 and G3 are a unit and have a different second color layout), said second unit being at a position apart from said first unit by two photoelectric converter element rows in the column direction (see Figure 2A; the ***two*** rows starting Y2 and G2 separate the aforementioned first and second units), said method comprising the steps of: classifying said

vertical charge transfer electrodes into sets each of which includes 16 vertical charge transfer electrodes as one set (see Figure 2A; *{There are two sets of 8 pulses (V1-V8) in the (m*n) set.}*, said 16 vertical charge transfer electrodes ranging from a first vertical charge transfer electrode to a 16th vertical charge transfer electrode succeeding one after another (see Figure 2A), and applying readout pulse voltages (see Figure 3, CCD Driver "3"; Col. 4, Lines 64-67) to said vertical charge transfer electrodes belonging to said photoelectric converter element row having said first color layout of said first unit (see Figure 2A, V1,V2 belonging to row starting C Y C), said first unit being selected from each said set (see Figure 2B, rows starting C1 and M1; *{Udagawa et al. is also a thin-out readout method (see Abstract, Lines 5,6.}*) and to said vertical charge transfer electrodes belonging to said photoelectric converter element row having said second color layout different from said first color layout of said second unit (see Figure 2A, V1,V2 belonging to C3; G3 and C3 row pair is different from C1 and M1), said second unit being formed in positions beginning at a position apart from said first unit by four photoelectric converter element rows in the column direction (see Figure 2A ; *{The row starting C1 (part of the first unit) and the row starting C3 (part of the second unit) are 4 rows apart, each from different units.}*) b) transferring the signal charge read out by said step a) through said vertical charge transfer channel regions for four photoelectric converter element rows in column direction (see Figure 2D; *{The jxn-row transfer operation transfers the addition of charges to a HCCD, which would have to be at least four photoelectric converter element rows apart from the row starting C1 according to Figure 2D.}*); c) applying readout pulse voltages (see Figure 3, CCD Driver "3"; Col. 4, Lines 64-67) to said vertical charge transfer electrodes belonging to said photoelectric converter element rows of said first and second units (see Figure 2B, V1-V4 of

rows starting C1 and M1 and V1-V4 of rows starting C3 and G3), which are not used to read the electric charge therefrom in said step a) (see Figure 2C, rows starting Y2,G2 and Y3,M3); and d) transferring the electric charge read out in said step c) and the electric charge read out in said step a) in said vertical charge transfer channel regions (see Figure 2C; Col. 4, Lines 36,37, "...VCCD.").

7. Claims 1-3,6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi et al. (US # 6,750,911).

As to claim **1**, Kobayashi et al. teaches a solid-state image pickup device (Figure 2), comprising: a semiconductor substrate (*The semiconductor substrate is an inherent part of a CCD.*) having a two-dimensional plane on a surface thereof (see Figure 2); photoelectric converter elements formed in or on said two dimensional plane in a matrix configuration having rows and columns (Figure 2; Col. 3, Lines 63-66), wherein (m*n) rows of said photoelectric converter elements form a set, where m and n are integers greater than one (Figure 6; *{M is 4 and n is 2; therefore making the set consist of the eight rows (R4 – G1) seen in Figure 6 (all columns not shown in Figure 6).}*); one vertical charge transfer channel region (Figure 2, vertical transfer register "20b") formed in said semiconductor substrate for each of the columns of said photoelectric converter elements, adjacent to said each column (Figure 2); two charge transfer electrodes so disposed over said vertical charge transfer channel regions for each of the rows of said photoelectric converter elements as to intersect said vertical charge transfer channel regions (Figure 6, V1, V3; *{The gates V1 and V3 are used for the single row of pixels starting with R4; pulses are applied to the row starting C1, so it is inherent that there is some sort of electrical*

connection disposed over the charge transfer region.}); an array of color filters formed above said photoelectric converter elements (Col. 3, Lines 63-67; Col. 4, Lines 1-7), said array including color filters of a plurality of colors arranged in a repeating pattern in the column direction (Figure 2; Figure 6; Col. 4, Lines 8-21), said repeating pattern comprising a unit of n rows (Figure 6, rows starting R4 and G4 are one unit; *{The rows starting R4 and G4 is an example of a unit. According to the definition in this claim, a unit can be any two rows.}*), and said color filters being formed in a one-to-one correspondence with said photoelectric converter elements (Figure 2; Figure 6); and a drive circuit capable of conducting a symmetric readout operation (see Figure 1, TG "22"; Col. 4, Lines 30,31) in each set of (m*n) rows of photoelectric converter elements, wherein rows read-out by said symmetric readout operation are symmetrically distributed in the column direction of said array (Figure 6; *{The rows starting R4 and G4 are rows read out by the symmetric readout operation as will be seen in the latter part of the claim. The rows are symmetric about the column direction where an axis of symmetry is defined as an axis between the rows R4 and G4, which defines a symmetry in the column direction.}*), said symmetric readout operation comprising: a first readout operation for reading first electric charges from a first group of photoelectric converter element rows which have an asymmetric distribution with respect to any one row of the first group (see Figure 6; *{The first **group** of rows are considered the rows starting with R4 and G4; furthermore, if the axis of symmetry were defined as the row starting G4, the distribution of this group would be considered asymmetric.).}*), into said vertical charge transfer channel regions (Col. 4, Lines 22-26); a jxn-rows transfer operation for transferring the readout first electric charge jxn rows after said first readout operation (Figure 6; *{As can be seen from Figure 6, the charges R4 and G4 are*

transferred 4 rows (j = 2, n = 2; j x n = 4) at time T4. Although they are transferred as the addition, the magnitude of the individual charges are transferred as is illustrated in Figure 6.}), where j is an integer greater than one, and a second readout operation for reading second electric charges from a second group of photoelectric converter element rows which have an asymmetric distribution with respect to any one row of the second group (Figure 6, *{The second* ***group*** *of rows are considered the rows starting R3 and G3; furthermore, if the axis of symmetry were defined as the row starting G3, the distribution of the group would be considered asymmetric.}*), at positions jxn rows downstream of the rows of said first readout operation (Figure 6, *{The row R1 (second readout operation) and the row G4 (first readout operation) are 4 rows downstream apart. The is true of the all the repeating sets of the CCD in the column direction starting with R1 and G4, making the second readout charges jxn rows downstream of the rows of said first operation (these rows being all the rows of the CCD starting G4).}*), into said vertical charge transfer channel regions (Figure 2, Figure 6; Col. 4, Lines 22-26), to respectively add the read-out second electric charges to the transferred first electric charges in said vertical charge transfer channel regions (see Figure 6, *{R4 (first readout operation) added to R3 (second readout operation). G4 (first readout operation) added to G3 (second readout operation).}*), each one of said read-out second electric charges being added to a respective one of said transferred first electric charges of a same color (Figure 6; Col. 6, Lines 18-35), said first and second readout operations being capable of reading electric charges from two rows of one unit of photoelectric converter element rows (see Figure 6; *{The first readout operation reads R4 and G4 which are two rows of one unit. The second readout operation reads R3 and G3, which are two rows of one unit.}*).

As to claim **2**, Kobayashi et al. teaches the solid-state image pickup device according to claim 1, wherein: said n is two; said j is m/2 (*see Claim 1; j and n have both been defined by examiner as 2 (j = m/2, where m = 4)*); and said symmetric readout operation reads two units per said set (see Figure 6, *{The units of R4, G4 (UNIT 1) and R3, G3 (UNIT 2) are read out every set.}*).

As to claim **3**, Kobayashi et al. teaches the solid-state image pickup device according to claim 2, wherein: said m is four (*see Claim 1; m has been defined by examiner as four*); said symmetric readout operation reads every second unit (see Figure 6; *{Every second unit would be either the odd or even numbered reds and greens. In either situation, the symmetric readout operation reads both.}*); said first readout operation reads a second row of a first unit and a first row of a second unit; and said second readout operation reads a first row of said first unit and a second row of second selected unit (Figure 6, *{Examiner interprets the first unit to be (G3 – 1st row; G4 – 2nd row) and the second unit to be (R4 – 1st row; R3 – 2nd row). There is no precedent in the claims that the units have to be adjacent.}*).

As to claims **6-8**, claims 6-8 are method claims corresponding to the apparatus claims 1-3, respectively. Therefore, claims 6-8 are analyzed and rejected as previously discussed with respect to the apparatus claims 1-3, respectively.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 12,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Udagawa et al. (see Patent Number above) in view of Tanaka et al. (US # 6,559,889).

As to claim **12**, Udagawa et al. teaches the solid-state image pickup device according to claim 11. The claim differs from Udagawa et al. in that it further requires a variable barrier formed in said semiconductor substrate below said photoelectric converter elements, said variable barrier being capable of modulating an amount of electric charge accumulable in each of said photoelectric converter elements.

In the same field of endeavor, Tanaka et al. teaches that the amount of signal charge accumulated in each sensor of a CCD array is determined by a potential barrier height (*Changing the barrier height changes or modulates the amount of charge received in the photosensors.*) of an overflow barrier that is formed in a p-type well region (see Figure 5, p-type well region "31"; see Col. 4, Lines 52-61) formed below the sensor section (see Figure 5, *{The only thing below the p-type region "31" is the n-type substrate; thus, the p-type well region has to be formed below the photosensors.}*). In light of the teaching of Tanaka et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor substrate of Udagawa et al. to include a p-type well region that determines the amount of charge accumulable in each photosensor, because one of ordinary skill in the art would recognize that this would allow the saturation signal charge amount to increase or decrease in anticipation of reduction, thereby preventing such characteristics as S/N ratio and dynamic from being deteriorated due to the reduction of saturation signal charge amount (see Tanaka et al., Col. 7, Lines 51-62).

As to claim **16**, Udagawa et al., as modified by Tanaka et al., teaches the method of controlling a solid-state image pickup device according to claim 15, wherein said device further comprises a variable barrier formed in said semiconductor substrate, said variable barrier being capable of modulating an amount of electric charge accumulable in each of said photoelectric converter elements (see Tanaka et al., Figure 5, p-type well region "31"; Col. 4, Lines 52-61) said method further comprising the step of x) modulating by said variable barrier an amount of electric charge accumulable in each of said photoelectric converter elements to one half of an original amount thereof before said step a) (see Tanaka et al., Col. 7, Lines 51-62; *{By increasing Vsub, the amount signal charge acumulable can be decreased. It is inherent in this system of Tanaka et al. that Vsub could be set to a value which allows the amount of charge to be decreased by one-half.}*).

Allowable Subject Matter

9. Claims 4,5,9,10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The reasons for indicating allowable subject matter can be found in the previous Office Action.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection for claims 1-3,6-8 presented in this Office action. The rejection of claims 11,12,15,16 stand. Accordingly, **THIS**

ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AD
8/5/05

NGOC-YEN VU
PRIMARY EXAMINER